CLAIMS

1. System for use in transmitting data and related control information from a first processing section to a second processing section, the first processing section being in a first clock domain, the second processing section being in a second clock domain, the system comprising:

a first logic section that may generate respective identification information that may be associated with and used to identify respective types of information represented by respective data and respective related control information; and

memory that may receive and store, at a first clock rate used in the first clock domain, the respective data and the respective related control information, the memory also storing, in association with the respective data and the respective related control information, the respective identification information generated by the first logic section that may be used to identify the respective types of information represented by the respective data and the respective related control information stored in the memory, the memory being configured to permit retrieval, at a second clock rate used in the second clock domain, of the respective data, the respective related control information, and the respective identification information stored in the memory.

2. The system of claim 1, wherein:

the respective data, when stored in the memory, is concatenated with the respective identification information that identifies the respective type of information represented by the respective data; and

the respective related control information, when stored in the memory, is concatenated with the respective identification information that identifies the respective type of information represented by the respective related control information.

3. The system of claim 1, wherein a second logic section in the second clock domain is configured to determine, based upon the respective identification information retrieved from the memory, respective further processing of the respective data and the respective control information retrieved from the memory.

4. The system of claim 3, wherein the respective identification information may indicate one of a respective type of control information, a respective type of address information, and user data.

5. The system of claim 1, wherein the first processing section includes at least one converter that may convert at least one bit stream into parallel words, the parallel words comprising the respective data and the respective related control information.

6. The system of claim 1, wherein the first processing section includes a plurality of converters that may convert respective bit streams into parallel words, the parallel words comprising the respective data and the respective related control information.

7. The system of claim 6, wherein the first processing section also comprises retimer circuitry that may be used to synchronize, based upon the first clock rate, transmission of the parallel words to the memory.

8. The system of claim 1, wherein the memory comprises a first-in-first-out memory.

9. The system of claim 7, wherein:

the plurality of converters comprises a first converter and a second converter;

the retimer circuitry comprises a first retimer circuit and a second retimer circuit;

the first retimer circuit is coupled to the first converter; and

the second retimer circuit is coupled to the second converter.

10. The system of claim 9, wherein:

the first converter receives a first bit stream;

the second converter receives a second bit stream;

the first converter is configured to generate, based upon the first bit stream, a first clock signal;

the second converter is configured to generate, based upon the second bit stream, a second clock signal;

the first retimer circuit receives the first clock signal; and

the second retimer circuit receives the second clock signal.

11. Method for transmitting data and related control information from a first processing section to a second processing section, the first processing section being in a first clock domain, the second processing section being in a second clock domain, the method comprising:

using a first logic section to generate respective identification information that may be associated with and used to identify respective types of information represented by respective data and respective related control information; and

receiving and storing in a memory, at a first clock rate used in the first clock domain, the respective data and the respective related control information, the memory also storing, in association with the respective data and the respective related control information, the respective identification information generated by the first logic section that may be used to identify the respective types of information represented by the respective data and the respective related control information stored in the memory, the memory being configured to permit retrieval, at a second clock rate used in the second clock domain, of the respective data, the respective related control information, and the respective identification information stored in the memory.

12. The method of claim 11, wherein:

the respective data, when stored in the memory, is concatenated with the respective identification information that identifies the respective type of information represented by the respective data; and

the respective related control information, when stored in the memory, is concatenated with the respective identification information that identifies the respective type of information represented by the respective related control information.

13. The method of claim 11, wherein a second logic section in the second clock domain is configured to determine, based upon the respective identification information retrieved from the memory, respective further processing of the respective data and the respective control information retrieved from the memory.

14. The method of claim 13, wherein the respective identification information may indicate one of a respective type of control information, a respective type of address information, and user data.

15. The method of claim 11, wherein the first processing section includes at least one converter that may convert at least one bit stream into parallel words, the parallel words comprising the respective data and the respective related control information.

16. The method of claim 11, wherein the first processing section includes a plurality of converters that may convert respective bit streams into parallel words, the parallel words comprising the respective data and the respective related control information.

17. The method of claim 16, wherein the first processing section also comprises retimer circuitry that may be used to synchronize, based upon the first clock rate, transmission of the parallel words to the memory.

18. The method of claim 11, wherein the memory comprises a first-in-first-out memory.

19. The method of claim 17, wherein:

the plurality of converters comprises a first converter and a second converter;

the retimer circuitry comprises a first retimer circuit and a second retimer circuit;

the first retimer circuit is coupled to the first converter; and

the second retimer circuit is coupled to the second converter.

20. The method of claim 19, wherein:

the first converter receives a first bit stream;

the second converter receives a second bit stream;

the first converter is configured to generate, based upon the first bit stream, a first clock signal;

the second converter is configured to generate, based upon the second bit stream, a second clock signal;

the first retimer circuit receives the first clock signal; and

the second retimer circuit receives the second clock signal.